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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
REILLY, SEAN M	
ART UNIT	**PAPER NUMBER**
2153	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/488,942	SHERER	
	Examiner	Art Unit	
	Sean Reilly	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-24 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-24, 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Another Examiner has been assigned to this application.

This Office action is in response to Applicant's amendment and request for reconsideration filed on March 28, 2006. Claims 18-24 and 29 are presented for further examination. Applicant's response, as submitted on September 25, 2006, to the rule 105 requirement is sufficient.

Response to Arguments

The majority of Applicant's arguments are moot in view of the new grounds of rejection set forth. This office action still utilized the combination of Metcalfe and AMD to reject the claim tree of claims 18-21 but using a different rationale for the combination.

In the sole remaining applicable argument, Applicant asserts that the Bentley cannot be properly combined with AMD because Bentley is used in a different field. Examiner respectfully disagrees. Both AMD and Bentley are concerned with the transfer of data between nodes and thus are analogous for at least this reason.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 18-24 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

With regard to claims 18-21 and 29, the preamble of claim 18 renders each claim indefinite. Applicant is attempting to claim an apparatus however the end of the preamble in claim 18 *recites the data comprising*. It is presumed that the claim should instead recite *the data communications adapter* at the end of the preamble.

With regard to claims 22-24, the use of the term "substantially" renders each claim indefinite. It is simply not clear when a set of bytes is *substantially equal* to another set of bytes. Thus, an artisan in the art would not be able to determine the metes and bounds of Applicant's claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 18-21 and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Metcalfe et al. (U.S. Patent 4,063,220; hereinafter Metcalfe) and AMD's Am79C830 FORMAC Plus as disclosed in "The SUPERNET 2 family for FDDI - 1991/1992 World Network Data Book" (hereinafter AMD) (Prior art submitted by applicant in parent application 09/028,088).

With regard to claim 18, Metcalfe disclosed a data communications adapter apparatus for coupling a host computer to a computer network employing communications media, the data comprising:

- Ethernet control circuitry (Figure 1, component 125);
- A host interface configured to exchange data with said host computer (Figure 1, component 125);
- A transceiver coupled to receive and transmit data over the media (Figure 1, component 211);
- Data transmit control circuitry responsive to said Ethernet control circuitry and couple to said transceiver, to said transmit data buffer, and to said host interface, for generating a packet transmit signal causing said transceiver to begin transmitting data from said transmit data buffer over said communications media (Figure 1, the transmitter logic sends data out of the output buffer);
- A receive data buffer coupled to said host interface (Figure 1, input buffer);

Metcalfe disclosed substantial features of the claimed ethernet card however, Metcalfe failed to disclose the early receive interrupt functionality. Nonetheless the use of an early receive interrupts was widely known in the art at the time of Applicant's invention, as evidenced by at least AMD. In an analogous art, AMD disclosed a communication adapter with a transceiver having a transmit buffer, a receive buffer, and a control circuitry [figure on page 2-4]. AMD further disclosed readout of a frame while it is being received to reduce delay in waiting for a complete frame [page 2-37, col.1 "Threshold Detection" paragraph]. The publication discloses interrupt circuitry [page 2-36, col.2 "Node Processor (NP) Interface"]. The publication discloses an early

receive interrupt once a predetermined number of bytes [threshold] of data packet less than all of said data packet has been received [Apparent from page 2-32 col.1 "INNTERRUPTS. The interrupt signals MINTR1 or MINTR2 ... are asserted when FORMAC Plus status changes", page 2-52 col.2 "The receive frames are loaded into the buffer memory ... for single-frame receive mode ... The RDATA timing depends upon the receive threshold value...", page 2-64 bottom of col.1 "the ST2 register contains status bit that may generate maskable interrupts on the MINTR2 pin", bottom of col.2 "Receive Frame. RSCVRM (bit10) - This bit is set, during single-frame receive-mode operation, to interrupt the NP and indicate that data is present in the buffer memory"].

Thus, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the use of an early receive interrupt, as disclosed by AMD, within Metcalfe's ethernet communication adapter, so that a host computer system can reduce processing time by passing the received bytes up to the application layer of the host system sooner (AMD, page 2-37, col.1 "Threshold Detection" paragraph).

As per claim 19, AMD disclosed that the AM79C830 is contained in a single application specific integrated circuit (ASIC).

As per claim 20, AMD disclosed the threshold is programmable [page 2-97 "Frame Threshold Register - FRMTHR"].

As per claim 21, AMD disclosed the circuit is programmable to generating a packet transmit signal when the buffer contains a predetermined number of bytes [page 2-98 col.1 "Transmit Threshold. XTHR"].

With regard to claim 29, Examiner takes official notice that it was widely known in the art at the time of Applicant's invention to use a ring buffer connected to the host interface via a DMA

channel for receiving data in on an ethernet adapter since both a ring buffer and DMA provide for the fast and efficient transfer and storage of data. Thus, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate a ring buffer receive buffer connected to the host interface via a DMA channel in order to provide for the fast and efficient transfer and storage of received data.

Claims 22 is rejected under 35 U.S.C. § 103 as being unpatentable over AMD and Kurio (U.S. Patent Number 5,774,640) and Bentley et al. (U.S. Patent Number 4,860,193; hereinafter Bentley).

As per claims 22, AMD discloses a method of transferring a packet of data comprising the steps of:

a) receiving from the communication media and storing in a receive buffer a first threshold number of bytes of the packet [page 2-37, col.1 "Threshold Detection"];

b) thereupon generating a first early interrupt from the adapter to the host computer [apparent from page 2-52 col.2 "The receive frames are loaded into the buffer memory ... for single-frame receive mode ... The RDATA timing depends upon the receive threshold value..."; page 2-64 bottom of col.1 "the ST2 register contains status bit that may generate maskable interrupts on the MINTR2 pin"; bottom of col.2 "Receive Frame. RSCVRM (bit10) - This bit is set, during single-frame receive-mode operation, to interrupt the NP and indicate that data is present in the buffer memory"];

c) thereafter receiving from the communication media and storing in the receive buffer a remainder of the packet [page 2-37, col.1 "Threshold Detection" - "...read out of the frame can then take place at the same time that the frame is being written"].

AMD does not specifically recite the host employing a driver allowing for early indication and having an early look ahead size. Nonetheless, as discussed above, AMD clearly disclosed the use of early receive interrupts to notify the host computer of the arrival of new data in the receive buffer upon reaching a threshold (or early look ahead size). In order for such an interrupt to be received at the host computer software level, the operating system must have a way to communicate and control the physical network card. It was notoriously well known in the art at the time of Applicant's invention that device drivers provided this missing interface so that the operating system could communicate with and configure/control a network card, as evidenced by at least Kurio Figure 4 and Col 7, lines 40-53. Thus, it would have been obvious to utilize a driver with the required functionality (e.g. the ability to receive interrupts and program the adapter card with a proper threshold or early look ahead size) within the system disclosed by AMD, in order to provide each host computer system the required functionality for utilizing a network card capable of the feature set disclosed by AMD.

AMD does not specifically teach adjusting the threshold or early look ahead size. However, AMD discloses the threshold is programmable (see page 1-2). Furthermore, in a similar field of endeavor, Bentley teaches adjusting the buffer threshold according to previous data block length to better adapt the buffer to the data length so as to reduce latency (see Abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to adjust the

threshold value based on packet length of received packet because it would have enabled the system to maintain data transfer rate at an optimal value.

Claims 23-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over AMD, Kurio, Bentley and further in view of Firoozman US patent 5,210,749.

As per claim 23, the publication does not disclose determining the threshold value based on the latency of the host computer and the network. In a similar field of invention, Firoozman teaches determining the threshold value based on the latency of the host computer and the network (col.14 lines 55-64). It would have been obvious for one of ordinary skill in the art to use Firoozman teaching with the Am79C830 publication because Firoozman teaches an improvement on the application of the Am79C830 chip (see col.1 lines 29-37).

As per claim 24, the amount of data in the buffer over the threshold equates to the interrupt latency (i.e. the amount of data being put into the buffer while the host computer is processing the early interrupt). Hence, it would have been obvious to take into account the amount of data in the buffer after the early interrupt was generated so as to adjust the threshold to compensate for the interrupt latency.

Conclusion

1. The prior art made of record, in PTO-892 form, and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Reilly whose telephone number is 571-272-4228. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glen Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 7, 2006

RUPAL DHARIA
SUPERVISORY PATENT EXAMINER